Low Voltage Electron Multiplying CCD in a CMOS Process

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ABSTRACT

Low light level and high-speed image sensors as required for space applications can suffer from a decrease in the signal to noise ratio (SNR) due to the photon-starved environment and limitations of the sensor's readout noise. The SNR can be increased by the implementation of Time Delay Integration (TDI) as it allows photoelectrons from multiple exposures to be summed in the charge domain with no added noise. Electron Multiplication (EM) can further improve the SNR and lead to an increase in device performance. However, both techniques have traditionally been confined to Charge Coupled Devices (CCD) due to the efficient charge transfer required. With the increase in demand for CMOS sensors with equivalent or superior functionality and performance, this paper presents findings from the characterisation of a low voltage EMCCD in a CMOS process using advanced design features to increase the electron multiplying gain. By using the CMOS process, it is possible to increase chip integration and functionality and achieve higher readout speeds and reduced pixel size. The presented characterisation results include analysis of the photon transfer curve, the dark current, the electron multiplying gain and analysis of the parameters' dependence on temperature and operating voltage.

Keywords: CCD, CMOS Image Sensors, Electron Multiplying Image Sensors, Low Light Imaging

1. INTRODUCTION

Images sensors such as Charge Couple Devices (CCDs) are well established for space imaging applications. The CCD has become a staple of high quality imaging in a range of different fields, providing good resolution, quantum efficiencies greater than 90%, high charge transfer efficiency and low readout noise[1]. Light-starved and high speed imaging applications such as Earth Observation and automated visual inspection benefit greatly from Time Delay Integration (TDI) and Electron Multiplication (EM) techniques, which are typically achieved using CCDs.

Electron Multiplication Charge Coupled Devices (EMCCDs) implement electron multiplication via the addition of gain elements into the CCD serial register, where the signal is amplified, thus improving the signal-to-noise ratio (SNR) even at high readout rates. With such improvements to the SNR, EMCCDs have the potential to achieve single photon detection. These image sensors are currently available commercially from e2v Technologies Ltd. and are growing in use in astronomical imaging. For comparison of the EMCCD with alternative low light imaging sensors, see papers[1-3].

1.1 CCDs

Modern scientific grade CCDs consist of a range of separate technologies from front-illuminated CCDs to thinned back-illuminated CCDs. Back-illuminated CCDs have become increasingly popular due to the improved quantum efficiency (QE) credited to a reduction in reflection and absorption losses and the thicker sensitive volume. Producing fully depleted sensors with thickness in excess of 100μm helps achieve very high QE spanning the visible and near infrared (IR) wavelengths.

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1.2 EMCCDs

Similar in structure to the CCD, EMCCDs have been commercially available for over a decade. The EMCCD has an additional multiplication register in between the serial register and the output amplifier. Electrons generated within the image area are transported to the multiplication register; where within each stage high clock voltages induce impact ionisation such that there is a small probability of generating secondary electrons. The gain per amplifying stage is usually small, of the order of a few percent, but an overall gain as high as several thousand can be achieved due to the large number of stages. The readout noise is effectively reduced by the multiplication gain and can be a fraction of one electron. With such noise reduction, the EMCCD can provide single photon imaging, and maintain the typical advantages of traditional CCDs, such as high QE and charge transfer efficiency, and low dark current.

1.3 CMOS Image Sensors

Active pixel CMOS image sensors (CIS) were developed later than CCDs, following from the great developments in deep submicron CMOS technology. CIS have become increasingly relevant within astronomical imaging and have already been implemented in several projects including the Ultra Violet Imaging Telescope (UVIT) of ASTROSAT[4]. CMOS sensors can provide a greater level of on-chip functionality, including signal processing and timing control. CIS devices usually have much lower power consumption than CCDs and should become increasingly dominant within the space industry when functionality and power are important considerations. Furthermore, due to the high charge to voltage factor (CVF) of the CMOS output buffers, CMOS sensors can exhibit much lower noise than high speed CCDs. Implementing techniques that are commonly seen in CCDs, such as TDI and EM within a CMOS image sensor should increase the performance so that a similar or greater functionality to CCDs is achievable. Constraints such as a lack of overlapping gates and the low supply voltages can be challenging especially when implementing electron multiplication.

2. THE EMTC1 DEVICE

The EM Test Chip 1 (EMTC1), shown in Figure 1, is the first image sensor to be designed at the Centre for Electronic Imaging (CEI) and aims to investigate EM in a low voltage CMOS process. The EMTC1 is a 4-phase buried channel CCD built using the 0.15µm, 6-level metal, 1.8/5V CMOS process by ESPROS Photonic Corporation (EPC)[5].

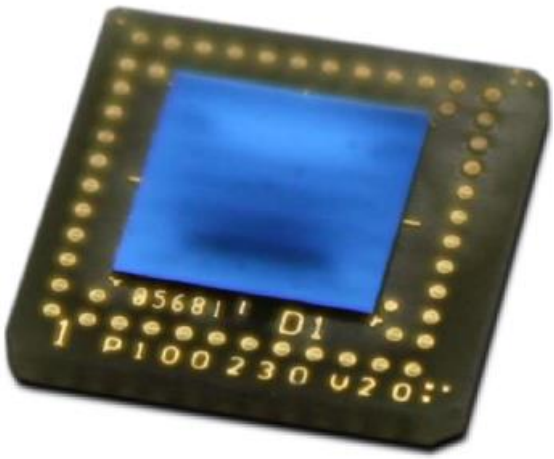

Figure 1: Photograph of EMTC1, flip-chip bonded to a ceramic carrier

The device is 50µm thick, back-illuminated and fully depleted, built on a high resistivity bulk silicon substrate. The EMTC1 has 200 (vertical) by 256 (horizontal) 10 µm square pixels, and operates with column-parallel readout. Each column has its own readout circuitry with two storage capacitors to help implement correlated double sampling (CDS). The CCD columns are grouped into 8 blocks of 32 columns and the readout is multiplexed 32-to-1 into 8 differential outputs, each carrying the stored reset and the signal samples from a block. The CDS is completed off-chip by subtracting the signal level from the reset level by differential amplifiers.

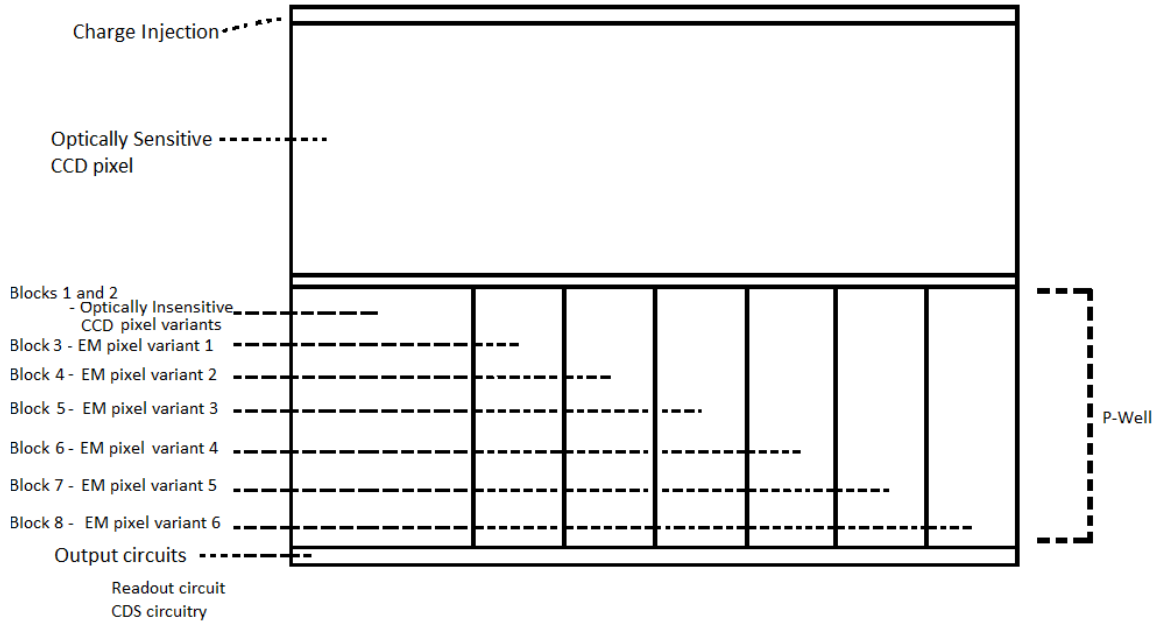

Figure 2: Block diagram of EMTC1

The top half of the array has a "classic" 4-phase CCD pixel structure. In the lower half, the leftmost two blocks of 32 columns are the same as the top half and serve as a reference, while the remaining 6 blocks implement different EM gate structures. Four of these have classic rectangular shape High Voltage (HV) gates, but vary slightly in the HV gate width and length. Blocks 7 and 8 (EM gates 5 and 6), contain two newly designed and recently patented HV gate shapes. These gates aim to increase the EM gain by increasing the electric field strength and electron concentration. The bottom half of the image array is shielded from direct charge collection by a p-well. The EPC process can realise inter-gate gaps of only 90 nm, and this helps in achieving high electric fields at a relatively low voltage. The gate oxide used in this 5V process does not break down until at least 15V. An initial Silvaco simulation in 3D was carried out to analyse the expected performance but only qualitative data could be obtained.

3. RESULTS

3.1 Device Characterisation

The device was characterised in the temperature range between 0°C and 25°C in vacuum, cooled by a two-stage Thermoelectric Cooler (TEC). The internal headboard could reach -20°C, however the insulating properties of the plastic socket in conjunction with the power dissipation of EMTC1 limited the minimum achievable device temperature to 0°C.

The device was clocked at a line rate of 10 kHz for a maximum frame rate of 25 fps if no overclock lines are included. Due to the charge shielding properties of the p-well, direct charge collection in the bottom half of the image area from light illumination over the whole device was found to be suppressed by a factor exceeding 72 dB.

3.2 Photon Transfer Curve

The Photon Transfer Curve (PTC)[6] is a commonly used technique to characterise the performance of an image sensor. Used predominantly to calculate the system gain, the PTC can also be used to calculate a number of parameters, including the CVF, the full well capacity (FWC) and the noise of the device.

The PTC was obtained here using light stimulus as signal. It is also possible to generate signal using dark current, however when using light stimulus, the dark current was minimised by cooling to 0°C. The PTC was obtained using frame differencing and is dominated by the shot noise of the signal. At very low signal levels the read noise floor, which is largely dependent on the on chip amplifiers, becomes visible.

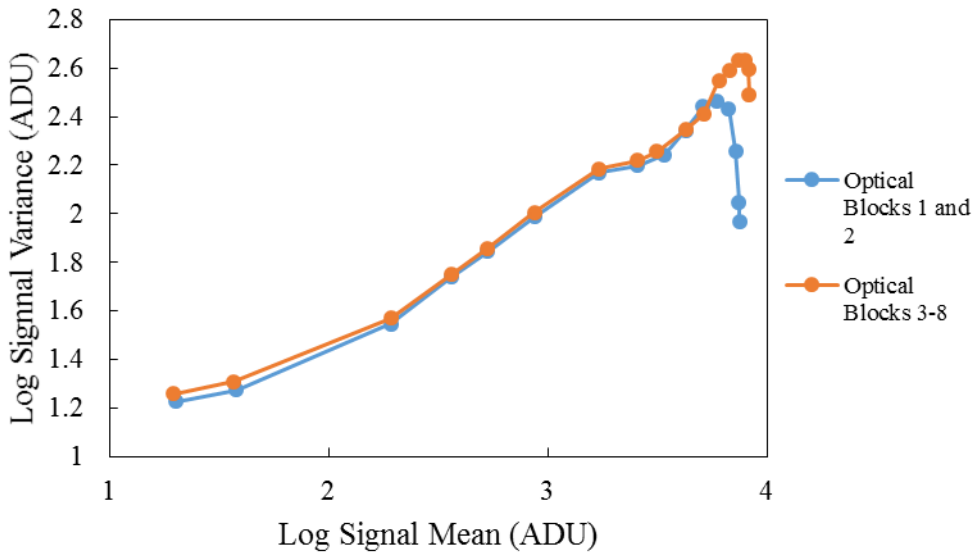

Figure 3: PTC produced using light stimulus as signal at 0°C

The PTC curve seen in Figure 3 analyses the optical regions of the device under light pulse stimulus and is representative for the of the PTCs produced for all blocks. The pixel non-uniformity has been removed by frame differencing and there is no fixed pattern noise.

The PTC is also useful in characterising the system gain, which describes the conversion of the collected photoelectrons to voltage at the amplifier's input. This value should be independent of the regions of the device because all columns use identical circuitry.

Table 1: The system gain of each region of the device

Pixel Region	System gain (e^-/ADU)
Shielded block 1 and 2	10.21 ±0.02
Optical block 1 and 2	9.34±0.02
3-8 (Shielded Whole EM)	12.21±0.02
EM Pixel 5	10.82±0.02
EM Pixel 6	10.88±0.02

As can be seen from Table 1, there is some variation in the conversion gain, which does not fall within the error. The cause of this variation between the regions could be attributed to an experimental error when calculating the system gain from the slope of the PTC at low signal levels. This variation within the gain needs further analysis; however an average gain of 10.01±0.02 e^-/ADU was used in the calculation and the analysis of the dark current.

3.3 Full Well Capacity

The FWC is the charge that an individual pixel can contain before saturation occurs. Several methods exists for the calculation of this device characteristic, however two methods were employed in the calculation of the results here:

1. FWC is the signal at which the device becomes non-linear to 5%
2. FWC is the signal corresponding to the peak of the variance in the PTC

Table 2: Full well capacity for each region of the device

Method	Optical CCD (e^-)	EM Whole (e^-)	EM Pixel 5 (e^-)	EM Pixel 6 (e^-)
1	72044.4 ±96.4	74967.3. ±92.8	73574.5. ±75.6	77876.1 ±119.5
2	80085.5 ±96.4	80085.9 ±92.8	80089.0 ±75.6	93167.5 ±119.5

There is some variation between the two methods of calculating the FWC, and the second method produces a higher value. Table 2 demonstrates that independently of the method of calculation, EM pixel 6 has the highest FWC and subsequently can hold the largest charge before saturation; EM pixel 5 and the entire EM region follow this closely. With a higher FWC, the greater the dynamic range of the device and the higher the possible signal within the device before saturation is reached.

3.4 Dark Current

The dark current of the device was measured over the temperature range from 0°C to +25°C. The dark current is due to the electrons thermally generated within the silicon substrate under dark conditions, and has strong temperature dependence. The dark current signal is of constant pattern and can be subtracted from the image signal level.

The statistical variations of the signal due to Poisson and readout noise were minimized by averaging 10 dark current images. Due to the internal power dissipation of EMTC1, the temperature of the device had to be measured accurately. To obtain the actual temperature of the silicon, a Pt100 sensor was glued to the surface of a separate device with identical power dissipation.

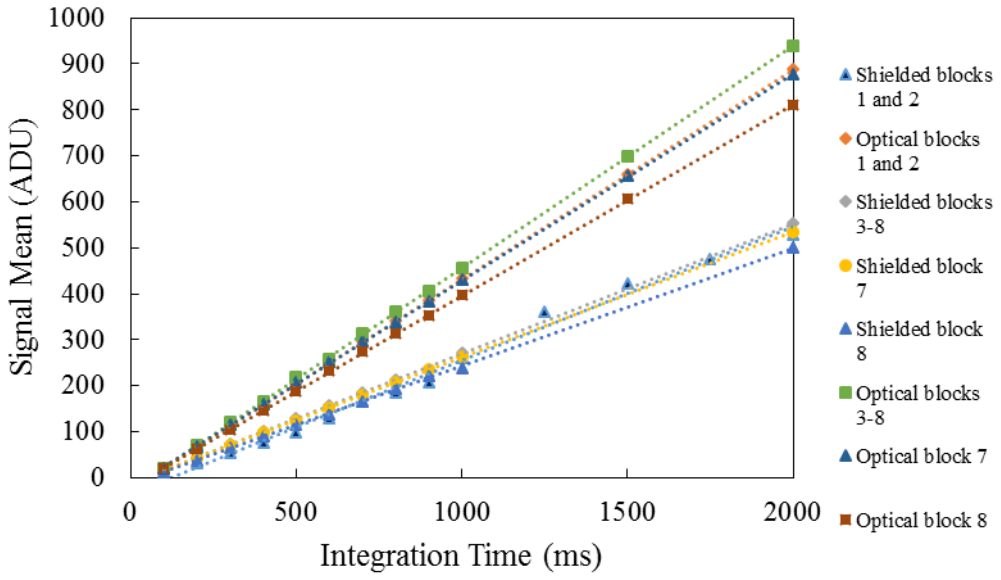

Figure 4: Dark current for each region of the EMTC1 at 0°C

For analysis of the sources of dark current within CCDs see paper[3,7], and further research has been completed studying dark current in CMOS devices[8] and EMCCDs[9]. Three sources are known to contribute to the total dark current within a CCD: the surface dark current generated at the interface between the silicon and silicon dioxide regions, the depletion dark current, and the dark current that has been generated within the field-free region, called the diffusion dark current. Furthermore when considering the EMTC1, it is important to note that one of the characteristics of non-inverted CMOS devices is the relatively high levels of dark current, usually an order of magnitude larger than those measured in CCDs[10]. The sources of the dark current within the EMTC1 have yet to be fully identifed and further research is required to determine these sources.

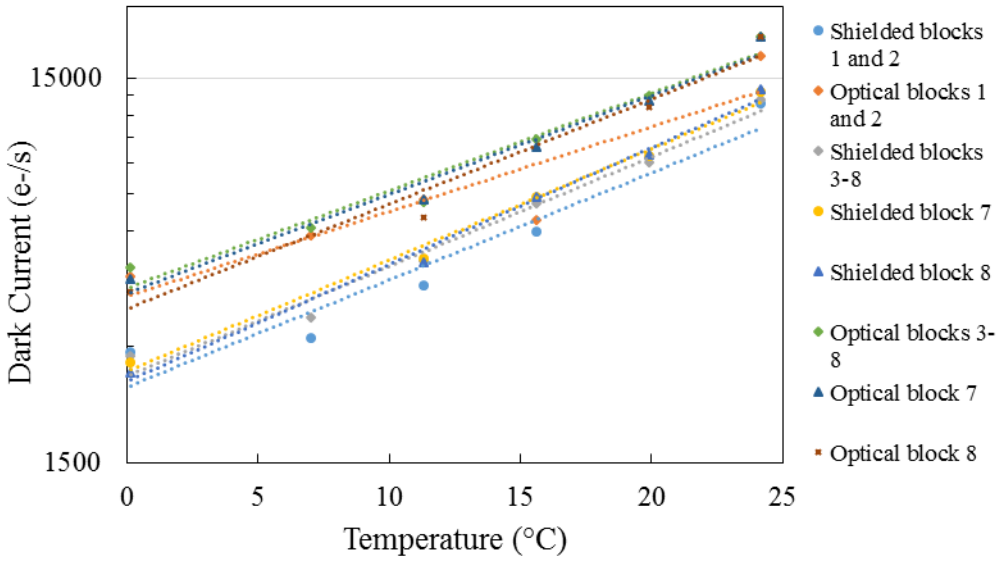

Figure 5: Dark current of EMTC1 over a range of temperatures.

Fig. 5 shows that dark current lines demonstrate the expected dependency of dark current on the temperature

$$DC = D_{FM} A T^3 \exp\left(-\frac{E_g}{2kT}\right) \quad (1)$$

where DC is the dark current, T is the operating temperature (K), E_g is the band gap energy and k is Boltzmann's constant. The proportionality constants in (1) are the pixel area A and the dark current figure of merit (D_{FM}) of the device. With pixel size constant across all blocks, the dark current variation between the different blocks is dependent on the D_{FM}.

It is well known that to effectively reduce the dark current the device should be cooled. If not cooled sufficently EMCCD systems can experience poor SNR especially when implemented in low light imaging. Due to the high dark current, the charge capacity available to the photo-charges is reduced and dark current non-uniformity can contribute to the fixed pattern noise.

Figure 5 shows the dark current for each region of the device. Testing demonstrated that there was a peak in the dark current at the transition between the EMCCD array and CCD array due to the p-well, which directs the current into the pixels above it. This increases the dark current average over the entire device. To remove this effect, the area of the device analysed did not include the edge pixels of any region. The optical regions of the device are seen to suffer from the highest dark current due to the charge collection from the whole depleted thickness of the device, followed closely by the shielded blocks 3-8 which consist of the EM pixel structures.

Table 3 draws a comparison between the dark current calculated for each region of the EMTC1 and the dark current from a commercially available e2v device. The back-illuminated CCD30-11 is a high performance sensor with an array of 1024 by 256 26µm square pixels. The dark current measurement quoted describes the devices under non-inverted mode operation.

Table 3: Dark current of two e2v CCD devices compared to each imaging region of EMTC1 at 293K

	EMTC1 Blocks 1-2 Non-Optical	EMTC1 Blocks 1-2 Optical	EMTC1 Blocks 3-8 Non-Optical	CCD30-11
Dark Current (e-/s/pixel)	8290	10296	9060	50000
Dark Current (nA/cm^2)	1.33	1.65	1.45	1.18

Early results predicted the dark current would greatly exceed that of similar devices; however, the dark currents for all device regions were similar to the CCD30-11. Blocks 3-8 of the EMTC1 containing the EM region had significantly higher dark current than the non-optical blocks 1-2 and the other CCD described. Hot pixels have been identified within the EM regions and could be the cause of the higher average dark current. The removal of their contribution to the analysis could result in a lower average dark current for the EM region. As can be seen from Figure 5, to reach dark current values suitable for low light imaging, the cooling will need to be greatly improved. Further reductions in the temperature should yield improved dark current and it is important to note that the integration time can be reduced further, potentially reducing the effect of the dark current.

3.5 EM Gain

EM gain was a major consideration in the design of the EMTC1. Utilising the additional EM register to increase the photon-generated charge above the readout noise is highly beneficial in low light level conditions. The EM gain occurs within the charge domain of the device before the charge to voltage conversion, and this results in an increase in the SNR. With high EM gain very fast readout is possible, which otherwise would have increased the amplifier noise significantly. The newly designed EM pixel variants aim to improve the EM gain by increasing the effective volume of the high field region and the electron concentration during the EM process. By implementing an optimised shape of the HV gate, the drop in electric field at the edges of the gate is reduced.

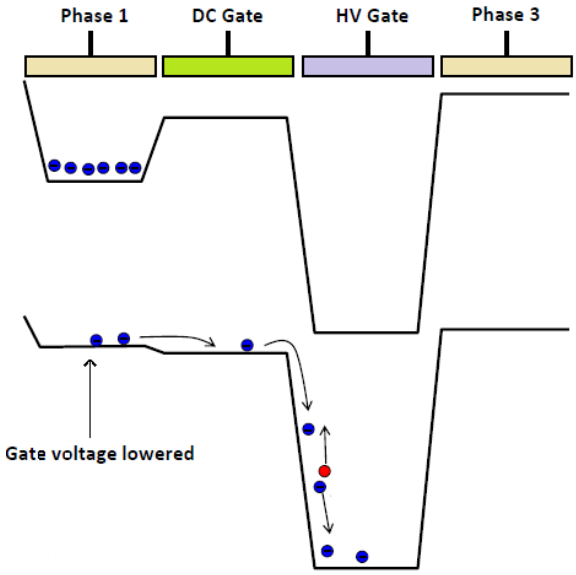

Figure 6: EM process within EMTC1

Figure 6 demonstrates the EM process within the EMTC1. Between the HV and DC gates, a region of high field above 10^5 V/cm is established. Electrons pass through this region and via impact ionisation electron-hole pairs are generated. A multiplication factor of around 1% per transfer is achieved, however to acquire a substantial gain, several hundred transfers are required. Within CCD processes, the HV voltage is usually greater than 40V. The CCD97, produced commercially by e2v, requires a voltage of 45V to produce significant gain.

By increasing the concentration of the electrons into a small volume, the charges can be corralled into an area of high field and the EM gain can be increased. To test the performance of these newly designed pixel variants the EM gain was measured here by taking the ratio between the signal with and without the avalanche gain applied over all 100 stages within the multiplication register.

Measurements were made when the device was illuminated with a stable light source with an input signal of ~1360 electrons and with an integration time of 100ms such that the dark current and thermal noise contributions were minimised. The EM gain was measured at 0°C while the HV voltage was increased from 3V to 15V. A HV voltage below 10V produced EM gain of 1, independent of the pixel varient tested.

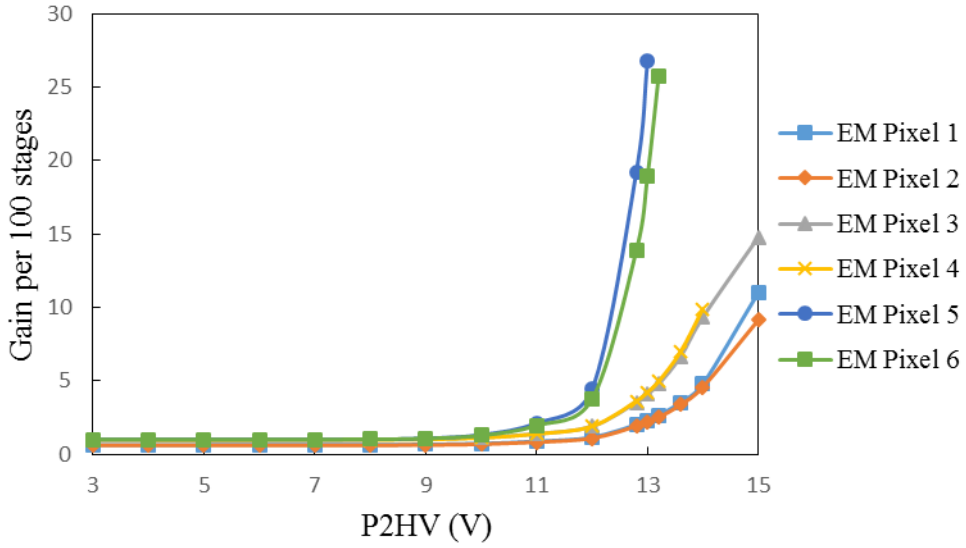

Figure 7: EM gain of EM pixels variants as a function of P2HV voltage at 0°C

Above a gate voltage of 10V the gain of the EM pixels 5 and 6 increased rapidly until the saturation of the output was reached at 13.0V for pixel 5 and 13.2V for pixel 6. While pixel 6 remained functional at a higher HV voltage, it did not reach the the peak gain experienced by pixel 5. The gain of the rectangular EM pixel variants (EM pixels 1-4) continued to grow but was unable to reach the same gain shown by the two newly designed pixels before the 15V HV limit was reached. These pixels, however were able to function effectively at higher voltage levels as saturation was not reached due to the lower gain. EM pixel variant 4 showed the highest gain among the rectangular designs, and reached saturation at 14V. From Figure 7 it was determined that the HV voltage at which all pixel variants worked under these conditions was 13.0V. A lower input signal would have produced a reduced output signal, however it would have allowed a higher voltage to be reached before saturation, and as such a potentially higher gain.

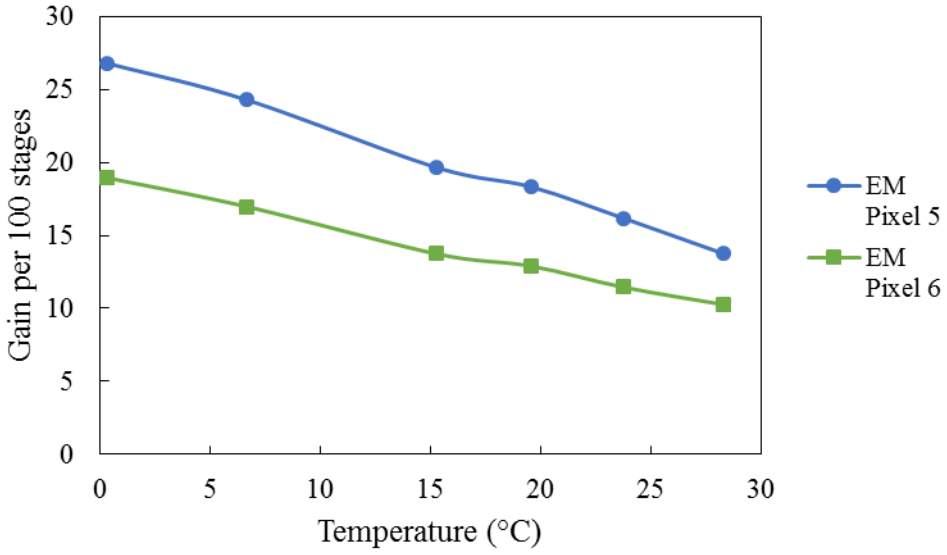

Figure 8: EM gain of pixel variants 5 and 6 as a funtion of temperature with HV=13V

The EM gain was then measured as a function of temperature between 0°C and 30°C, and demonstrated the expected temperature dependence. As temperature is increased, the probability that a primary electron will generate a secondary electron within the silicon is reduced, reducing the EM gain.

The gain demonstrated by EM pixels 5 and 6 is approximately 3% per a stage at HV=13V. Commercially available e2v EMCCDs, such as CCD97, achieve gain of ≈1.5% per stage with a HV voltage of 45V. Our new EM gain elements are able to produce a gain twice that of current EMCCD devices at less than a third of the voltage required by CCDs, which is welcome news for the development of low power EM imaging systems.

The effect of concentrating the charge into a high field area does improve the gain compared to traditional rectangular gate structures, however there may still be losses of the field at the edges effecting the strength of the field and hence the probability of secondary electron generation. Further testing of the EM gain of the new gates is required and an analysis of the EM ageing properties of the device will provide insight into the gain stability and lifespan of the EMTC1.

4. CONCLUSIONS

In conclusion, the paper has presented early characterisation results of the newly designed EMTC1. The results have demonstrated that the dark current is of a similar magnitude seen in commercially available devices, however the EM region experienced a higher dark current than the non-EM blocks. This difference can potentially be attributed to hot pixels within the EM region.

EMCCD structure in a CMOS process has been demonstrated and the EM gain has been found to be quite high. Furthermore, the two newly designed EM pixels have demonstrated higher gain than seen in traditional rectangular gate shape pixels. The EM gain produced by the EM pixels 5 and 6 is twice that possible in many commercially available EMCCDs and can be achieved with a HV less than third that of traditional devices. Further testing will be required at lower temperatures to fully characterise the device and explore the EM gain of the new elements.

The device also has a number of other features including fully depleted 50µm thick silicon and back illumination, so there is a possibility of X-ray and near-IR imaging. Further device characterisation is required, including charge transfer inefficiency, quantum efficiency and EM ageing measurements, to fully quantify the device's parameters.

The aim of this device was to test the potential for several new technologies and their applicability for space and astronomical imaging, and while further characterisation is required, these results demonstrate that the technology is not only functional but producing EM gain that greatly exceeds that of similar devices.

REFERENCES

[1] Djazovskia, O., Daigleb, O., et al, "Electron-Multiplying CCDs for Future Space Instruments," Proc. SPIE 8915, 89150Q (2013).

[2] Daigle, O., Carignan, C. and Blais-Oullette, S., "Faint flux performance of an EMCCDS," Proc. SPIE 6276, 62761F (2006).

[3] Dussault, D. and Hoess, P., "Noise performance comparison of ICCD with CCD and EMCCD cameras," Proc. SPIE 5563, 195 (2004).

[4] Kumer, A., Ghosh, S.K., Hutchings, J., et al, "Ultraviolet imaging telescope (UVIT) on ASTROSAT," Proc. SPIE 8441, 84421N-1 (2012).

[5] ESPROS Photonics corporation, 2015, http://www.espros.com/ (13/06/2016).

[6] Janesick, J., [Scientific Charge-Coupled Devices], SPIE Press, Washington USA, (2001).

[7] Widenhorn, R., et al, "Temperature dependence of dark current in a CCD," Proc. SPIE 4669, 193-201 (2002).

[8] Porter, W., et al, "Dark Current Measurements in a CMOS Imager", Proc. SPIE 6816, 68160C-1 (2008).

[9] Smith, D.R., Ingley, R. and Holland, A.D., "Proton Irradiation of EMCCDs", IEEE. Transactions on Electron Devices 53(2), 205-210 (2006).

[10] Cheng, H.Y. and King, Y.C., "An ultra-low dark current CMOS image sensor using n+ ring reset", IEEE Electron Device Lett 23, 538-540 (2002).